the recessed nitride liner being dimensioned and configured to prevent hot carrier effects due to charge trapping for charge which traverses a channel of the transistor;

an oxide fill disposed above said nitride liner, such that said oxide fill extends above and below the uppermost surface of said nitride liner substantially to a top surface of said substrate and completely filling below the uppermost surface, respectively; and

the oxide fill is disposed above said liner such that polysilicon material used in other processing is prevented from entering the trench.

REMARKS

This application has been reviewed in light of the Office action dated October 15, 1999. Claims 1-5, 7 and 24 and 25 are pending in the application. Claims 8 and 10 have been canceled without prejudice. Claims 1 and 24 have been amended to further clarify the invention. No new matter has been added by the amendments. The Examiner's reconsideration of the rejection in view of the amendments and the following remarks is respectfully requested.

By the office action, claims 1-5, 7, 8, 10, 24 and 25 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Fukuda (Japanese Patent No. 57-159038 hereinafter Fukuda) in view of Lou et al. (U.S. Patent No. 5,872,045, herein after Lou) and Wolf. Claims 8 and 10 have been canceled without prejudice.

The Examiner stated that Fukuda discloses a trench isolation structure in FIGS. 4a-4e of Fukuda which includes the elements of the present invention. The Examiner also stated that since shallow trench isolation regions extend below 5000-8000 angstroms as disclosed by Wolf, the present invention is obvious over the references. The Examiner cited Lou to show that polysilicon may be used to provide isolation.

Fukuda is directed to a method for forming V-shaped isolation regions. A translation of Fukuda has be obtained and is enclosed herewith for the Examiner's convenience. It appears that Fukuda fills a trench with polysilicon material and provides improved isolation by forming a nitride isolation layer 12' into a p-doped region. The nitride layer 12' remaining in the trench

provides extra isolation between portions of an N-doped well in substrate 10. Fukuda provides isolation between structures by including a V-shaped groove which extends into a p-doped region below the n-doped region of substrate 10. Instead of counter-doping polysilicon in the p-doped area of substrate 10 (which forms an inversion region), a nitride layer is formed in the p-doped area to provide better isolation between adjacent laterally disposed structures (i.e., structures in the trench on opposing sides of the trench). As is known in the art, a P-well is generally located a greater depth in a substrate than the P-well (see e.g. Lou, FIG. 2).

Fukuda employs a V-groove by etching substrate 10 along crystal planes of silicon (see translated copy of Fukuda page 1). If etching is continued, the V- groove will open up further making the trench wider. Therefore, Fukuda would not want to extend the trench further down into the substrate then the minimum amount necessary to conserve layout area. Instead, Fukuda attempts to just reach the p-doped region. To prevent the undesirable alternative of N-inversion region formed by contra-doping silicon in the lower portion of the trench, a nitride layer is formed extending above the p-doped region to provide isolation laterally across the trench.

The polysilicon of Fukuda does not include a conductive component as previously believed by the Applicant. It appears that the polysilicon remains <u>undoped</u> and acts as an isolation region. Further, as shown by Lou, isolation regions may include <u>undoped</u> polysilicon. The cited references taken as a whole, however, fail to teach or suggest a nitride liner recessed within a trench and <u>an uppermost surface</u> of said nitride liner being disposed <u>just below</u> a transistor channel depth, Dc, of a transistor disposed in a well beside said shallow trench isolation structure, the recessed nitride liner being <u>dimensioned and configured</u> to prevent hot carrier effects due to charge trapping for charge which traverses a channel of the transistor.

The present invention, as amended, includes, *inter alia*, a nitride liner recessed within a trench ... <u>an uppermost surface</u> of said <u>nitride liner</u> being disposed <u>just below a transistor channel depth, Dc</u>, of a transistor disposed in a well beside said shallow trench isolation structure, the recessed nitride liner being <u>dimensioned and configured</u> to prevent hot carrier effects due to charge trapping for charge which traverses a channel of the transistor.

Claim 1 and claim 24 have been amended to more positively recite the structure of the invention. It is clear the Fukuda does not contemplate hot carrier effects or charge trapping of a nitride liner in a trench. Fukuda attempts to provide a more complete isolation between adjacent regions by extending the isolation trench into the p-doped region. The nitride dielectric 12' in Fukuda must extend above the n-doped region to achieve better isolation. Lou represents that a trench may be filled with undoped poly as a substitute for silicon dioxide. Lou, in FIG. 2, also shows trench isolation regions extending into a p-doped substrate 12 from an n-doped portion of substrate 11. Wolf discloses trench isolation regions extending up to 8000 angstroms into a substrate. However, even if these references are combined, a trench isolation region having a nitride liner recessed within the trench ... an uppermost surface of said nitride liner being disposed below a transistor channel depth, Dc, of a transistor disposed in a well beside said shallow trench isolation structure, the recessed nitride liner being dimensioned and configured to prevent hot carrier effects due to charge trapping for charge which traverses a channel of the transistor is not taught or suggested.

If the references are combined, the resultant structure would include a trench isolation structure extending down to a p-doped region (to a depth of between 5000 to 8000 angstroms) with a nitride layer formed in the p-doped region portion of the trench. The combined structure would not include an uppermost surface of said nitride liner being <u>disposed just below a transistor channel depth</u>, Dc, of a transistor disposed in a well beside said shallow trench isolation structure, the recessed nitride liner being <u>dimensioned and configured</u> to prevent hot carrier effects due to charge trapping for charge which traverses a channel of the transistor. The nitride liners of Lou and/or Fukuda are not <u>dimensioned and configured</u> to prevent hot carrier effects due to charge trapping for charge which traverses a channel of the transistor. The nitride layer is limited to a bottom portion of the trench and does not have the benefits afforded the present invention in terms of protection of silicon surfaces of the sidewalls of the trench which is one reasons for the inclusion of the nitride liner (see e.g., the Background of the present invention). In addition, the

structure of Lou may be subjected to the charge trapping which the present invention seeks to avoid.

The Examiner gives no patentable weight to what he contends is functional language. However, a claim containing a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus if the prior art apparatus teaches all the structural limitations of the claim. *Ex Parte Mashum*, 2 USPQ 2d 1647, 1987. Even if the prior art device performs all the functions recited in the claim, the prior art cannot anticipate the claim if there is any structural difference. *In re Ruskin*, 347 F.2d 843, 1965. It is respectfully submitted, that the uppermost surface of the nitride liner and where it is placed is **structure**. The liner is dimensioned and configured to prevent hot carrier effects due to charge trapping. Further, a transistor depth, Dc is a limitation for the uppermost surface of the nitride liner which is not disclosed or suggested by the prior art references. This structure is not disclosed or suggested by the prior art references, either alone or in combination.

The Examiner contends that the nitride liner of Fukuda and the fact that isolation regions can extend to 8000 angstroms is sufficient to render the invention obvious. The location of the uppermost surface of the nitride liner is not merely a design choice, as the Examiner contends. Instead, the cited references do not even suggest hot carrier effects and charge trapping of a nitride liner, let alone, disposing an uppermost surface of the nitride liner just below a channel depth. Claims 1 and 24 have been rewritten in part to further clarify the structural differences between the present invention and the prior art.

The afore-mentioned fundamental differences between Fukuda, Lou and Wolf and the presently claimed invention provide sufficient basis to reverse this rejection and allow the claims of the present invention. The cited references either alone or in combination do not teach or suggest a shallow trench isolation including, *inter alia*, an uppermost surface of said nitride liner being disposed just below a transistor channel depth, Dc, of a transistor disposed in a well beside said shallow trench isolation structure, the recessed nitride liner being dimensioned and configured to prevent hot carrier effects due to charge trapping for charge which traverses a channel of the

transistor. Accordingly, withdrawal of the rejection of claims 1-5, 7 and 24 and 25 is respectfully requested for at least the reasons stated.

In view of the foregoing amendments and remarks, it is respectfully submitted that all the claims now pending in the application are in condition for allowance. Early and favorable reconsideration of the case is respectfully requested.

Respectfully submitted,

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SPECIFICATION

1. TITLE OF INVENTION

Method for Forming V-Shaped Isolation Region

2. CLAIM

A method for forming a V-shaped isolation region, comprising the steps of forming a groove that is V-shaped in cross-section in a semiconductor substrate to a depth which reaches at least to the p-type semiconductor region, and then sequentially forming a silicon oxide film and a silicon nitride film on the side walls of said V groove, and then removing the silicon nitride film inside said V groove and leaving only [the portion] near the bottom of said V groove, and then filling the V groove with polycrystalline silicon.

3. DETAILED DESCRIPTION OF THE INVENTION

The present invention pertains to forming a V-type isolation region on a semiconductor substrate. More specifically, it pertains to forming a V-type isolation region in which an n-type inversion layer does not occur in the p-type substrate region near the bottom of the V groove.

When forming a bipolar integrated circuit, a groove that is V-shaped in cross-section is generally formed in the <110> direction in substrate crystal whose principal plane is the {100} plane. The object of this V groove is to isolate the n-type layer on the substrate surface, so it is formed to a depth which reaches the underlying p-type region.

On the other hand, this V groove is filled with polycrystalline silicon (hereinafter abbreviated "poly Si") in order to flatten the substrate surface, and a silicon dioxide (SiO_2) film is provided between the V groove side wall and the poly Si.

In this sort of structure, if the SiO_2 film which makes contact with the p-type substrate is doped with Na^+ ions, an n-type inversion region occurs in the p-type region, and isolation between device regions becomes incomplete. A method of preventing this is to make the region which contacts the V groove bottom p^+ and avoid the formation of an inversion region, but a simpler method is to cover the surface of the SiO_2 film in the V groove with a silicon nitride (Si_3N_4) film and block the Na^+ ions.

This method encounters the following sorts of problems. As shown in FIG. 1, n-type layer 2 is atop p-type silicon substrate (hereinafter abbreviated "Si substrate") 1, and a V groove is formed in this, and its side walls are coated with SiO_2 layer 3. When Si_3N_4 film 4 is additionally applied and formed atop this, continuous from the substrate's horizontal surface to the sides of the V groove, if the Si_3N_4 film on the substrate's horizontal surface portion is removed in order to form devices the Si_3N_4 film is etched too much as shown in FIG. 2 and small groove 7 forms. This sort of small groove causes breaks in the wiring layer and other problems, so formation thereof must be avoided at all costs.

Similarly, if an end is formed in the Si_3N_4 film at the horizontal portion as shown in FIG. 3, this causes overhang 7', and causes wiring breaks. Furthermore, in the drawings 5 is poly Si and 6 is an SiO_2 region formed on the surface thereof.

Therefore, when blocking Na^+ ions by means of an Si_3N_4 film, it is necessary to form it only at the required portion and in such a manner that it does not extend to the substrate surface.

Also, in the exposure system known as proximity, it is possible to provide a mask a few μ away from the photosensitive layer, and it is also possible to transfer a sharp image. Also, thanks to advances in positioning art, a positioning margin of 1 μm is not that severe a condition.

Therefore the present invention utilizes this sort of exposure art to selectively form an Si_3N_4 film about 3 μm wide in the horizontal direction in a V groove about 6 μm wide. That is, the present invention is characterized by forming a groove that is V-shaped in cross-section in a semiconductor substrate to a depth which reaches at least to the p-type semiconductor region, and then sequentially forming an SiO_2 film and an Si_3N_4 film on the side walls of the V groove, and then removing the Si_3N_4 film inside the V groove and leaving only [the portion] near the bottom of the V groove, and then filling the V groove with poly Si.

FIG. 4 shows these steps in one embodiment of the present invention. First, as shown in FIG. 4(a), the surface of Si substrate 10 is coated with SiO_2 film 11 and Si_3N_4 film 12, and V groove formation window 13 is opened. Next, after the V groove is formed by etching, the surface inside the groove is covered with SiO_2 film 11' (FIG. 4(b)). If this SiO_2 film 11' is formed by thermal oxidation, a CVD SiO_2 film is formed atop the previous Si_3N_4 film 12, resulting in a 3-layer pattern of $SiO_2/Si_3N_4/$ CVD SiO_2. When patterning the Si_3N_4 film formed subsequently, this protects Si_3N_4 film 12. Also, this is not shown in the drawings, but of course the V groove is formed to a depth which reaches the p-type region in the substrate.

Next, after Si_3N_4 film 12' is coated and formed on the substrate's entire surface, photoresist is applied, and a noncontact exposure system such as the proximity system is used so that photoresist 14 remains only in the bottom of the V groove. This sequence is shown in FIG. 4(c). Next, photoresist 14 is patterned into a mask by dry etching, and the Si_3N_4 film is removed from areas other than the bottom of the V groove. FIG. 4(d) shows this state.

Dry etching can be adapted to the material being etched by parameter adjustment, so utilizing this makes it possible to pattern the Si_3N_4 film with the photoresist as a mask. If the SiO_2 film on the V groove side walls is a two-layer CVD film/thermal oxidation film, this etching step removes to the CVD SiO_2 film.

After this it is time to start the step of forming a normal V groove poly Si isolation region: the interior of the V groove is filled with poly Si, and the surface is polished flat, and the poly Si surface is oxidized and covered with an SiO_2 layer (FIG. 4(e)).

As explained above, the inventive method can cover the bottom of the V groove with an Si_3N_4 film that is not connected to the Si_3N_4 film on the surface of the substrate. This prevents the formation of an n channel at the V groove isolation filled with poly Si.

4. BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 through FIG. 3 show prior art. FIG. 4 is a drawing showing an embodiment of the present invention. In the drawings, 1 is the Si substrate p-type region, 2 is the Si substrate n-type region, 3 and 6 are SiO_2, 4 is Si_3N_4, 5 is polysilicon, 7 is the groove, 7' is the overhang, 10 is the Si substrate, 11, 11', and 11" are SiO_2, 12 and 12' are Si_3N_4, 13 is the etching window, and 14 is photoresist.

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FIG. 1 ~ FIG. 4